In the Claims

1(Currently Amended). A clocking system for a memory, comprising:

an external clock;

a clock shaper having an input coupled to the external clock and an access clock at an output, the access clock clocking the memory;

a first delay block having an input coupled to the external clock and an output coupled to a master of an output register;

a slave of the output register coupled to the external clock; and

a second delay block having an input coupled to the external clock and an output coupled to the slave of the output register.

2(Cancelled).

3(Previously Presented). The system of claim 1, wherein a first delay by the first delay block is not equal to a second delay by the second delay block.

4(Original). The system of claim 3, wherein the first delay is greater than the second delay.

5(Original). The system of claim 1, further including a logic inversion stage coupled between the output of the first delay block and the master of the output register.

6(Original). The system of claim 1, wherein the clock shaper is a programmable clock duty cycle control block.

7(Original). The system of claim 1, wherein the first delay block has a programmable delay.

8(Previously Presented). The system of claim 1, wherein the second delay block has a programmable delay.

9(Original). A method of operating a clocking system for a memory, comprising the steps of:

a) splitting an external clock into a plurality of clock lines;
b) shaping one of the plurality of clock lines to form an access clock;
c) delaying a second of the plurality of clock lines to form a master clock;
d) coupling the master clock to a master of an output register;
e) delaying a third of the plurality of clock lines to form a slave clock; and
f) coupling the slave clock to a slave of the output register.

10(Original). The method of claim 9, wherein step (a) further includes the step of:

a1) shaping an outside clock to form the external clock.

11(Original). The method of claim 9, wherein step (c) further includes the step of:

c1) determining a desired delay for the second of the plurality of clock lines.

12(Original). The method of claim 9, wherein step (f) further includes the steps of:

f1) determining if a minimum clock-to-data valid time is desired;
f2) when the minimum clock-to-data valid time is desired, setting a slave delay to a minimum.

13(Original). The method of claim 12, further including the steps of:

f3) determining a minimum clock-to-data valid time;
f4) setting a clock speed to a maximum clock speed;

14(Original). The method of claim 13, further including the steps of:

f5) determining a clock-to-data margin at a slow corner;
f6) increasing a master delay by the clock-to-data margin.

15(Original). The method of claim 14, further including the step of:

f7) adjusting the master delay to provide an equal failure rate for a required clock-to-data time and a required cycle time.

16(Withdrawn). A memory system comprising:

a memory core;
a memory address coupled to the memory core and having an access clock; and
a master and slave output register coupled to the memory core, wherein a master portion and a slave portion of the master and slave output register are both in a transparent state during a part of a read operation.

17(Withdrawn). The memory system of claim 16, further including a master clock coupled to the master portion of the master and slave output register.

18(Withdrawn). The memory system of claim 17, further including a slave clock coupled to the slave portion of the master and slave output register.

19(Withdrawn). The memory system of claim 18, wherein the master clock and the slave clock have the same period.

20(Withdrawn). The memory system of claim 19, wherein the master clock is out of phase with the slave clock.